

VLSI Design

Lecture 12: Transistor sizing

Shaahin Hessabi

Department of Computer Engineering

Sharif University of Technology

Adapted, with modifications, from lecture notes prepared
by the author (from Prentice Hall PTR)

Topics

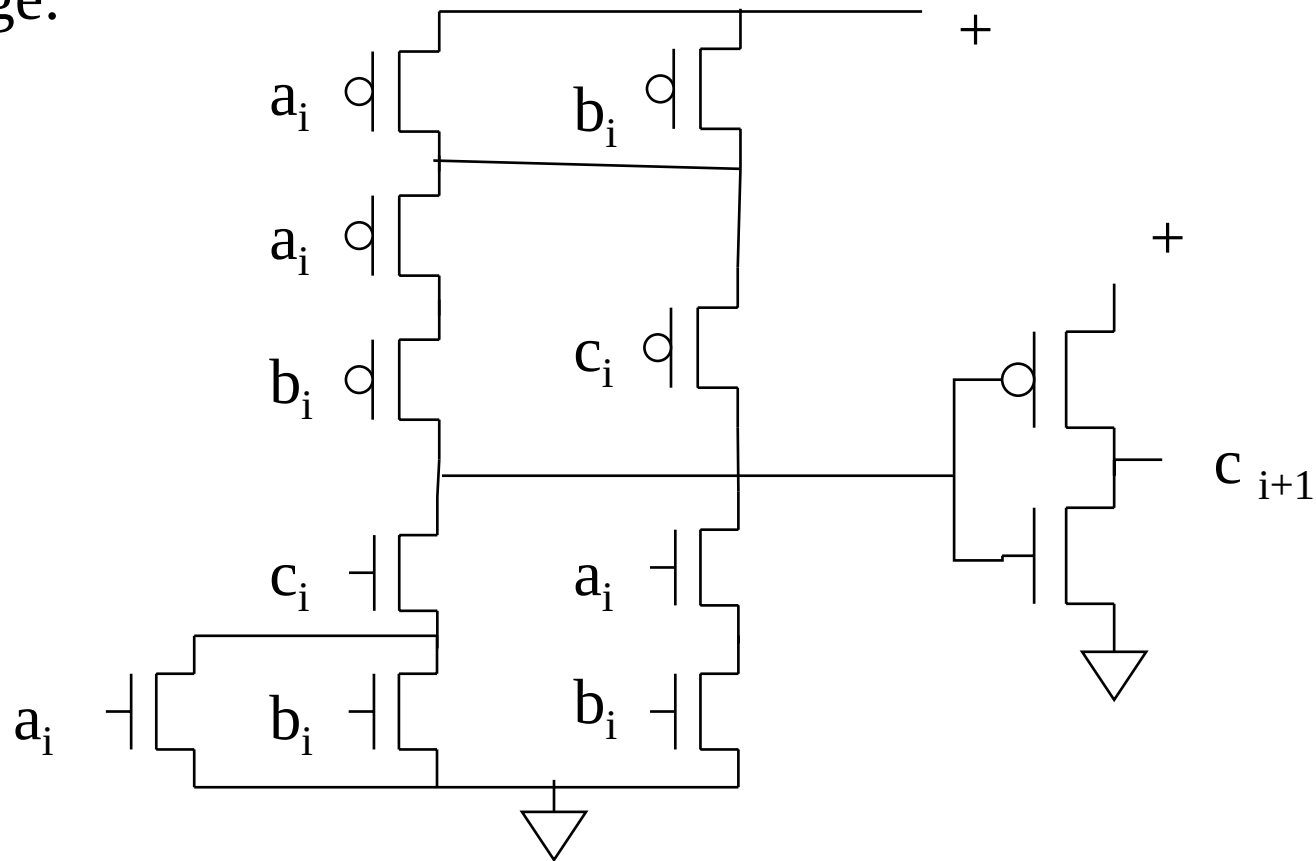
- Transistor sizing:
 - Spice analysis.
 - Logical effort.

Transistor sizing

- Not all gates need to have the same delay.
- Not all inputs to a gate need to have the same delay.
- Adjust transistor sizes to achieve desired delay.

Example: adder carry chain

One stage:

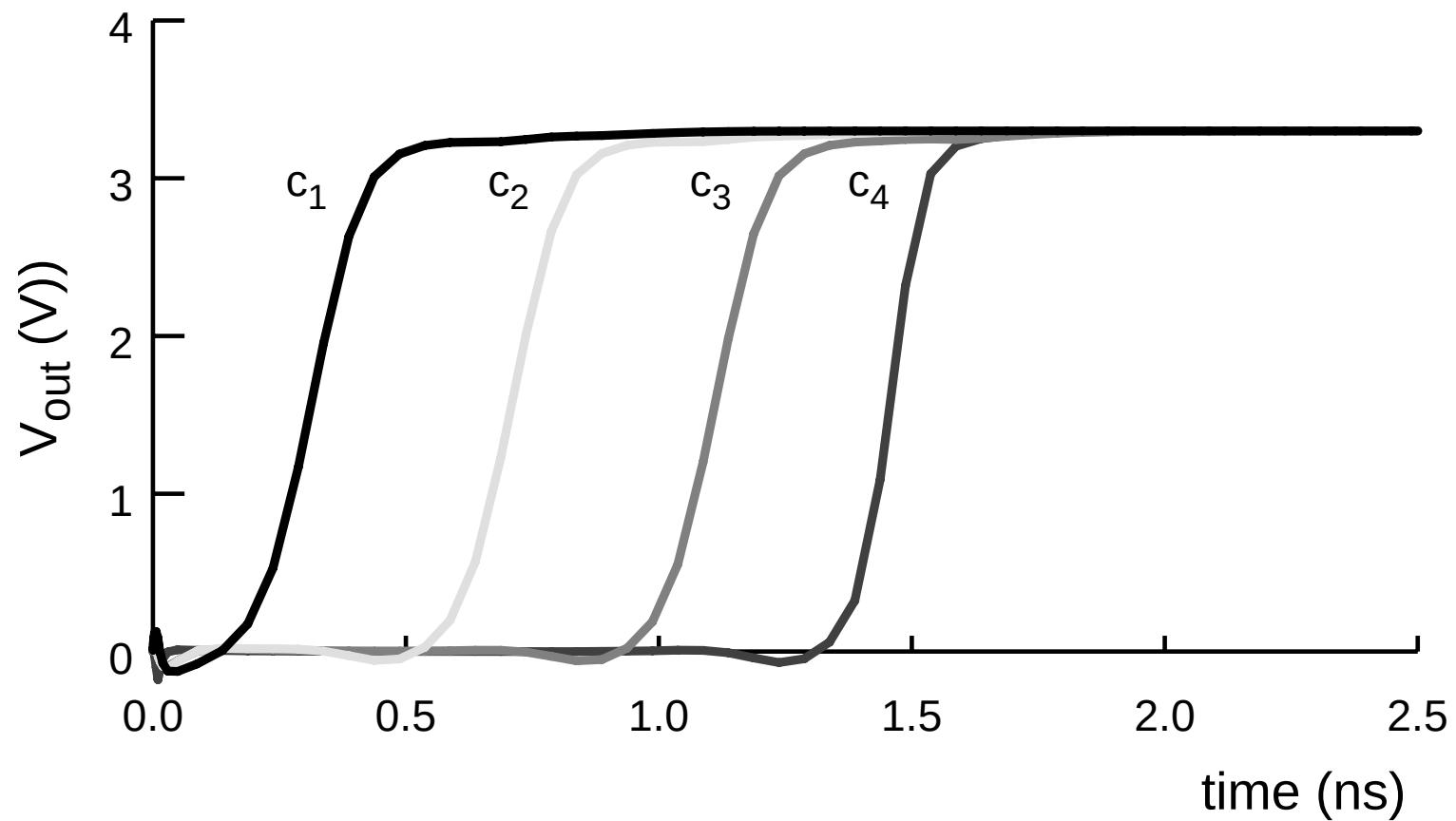


Carry chain optimization

- Connect four stages.
- Optimize delay through carry chain by selecting transistor sizes.

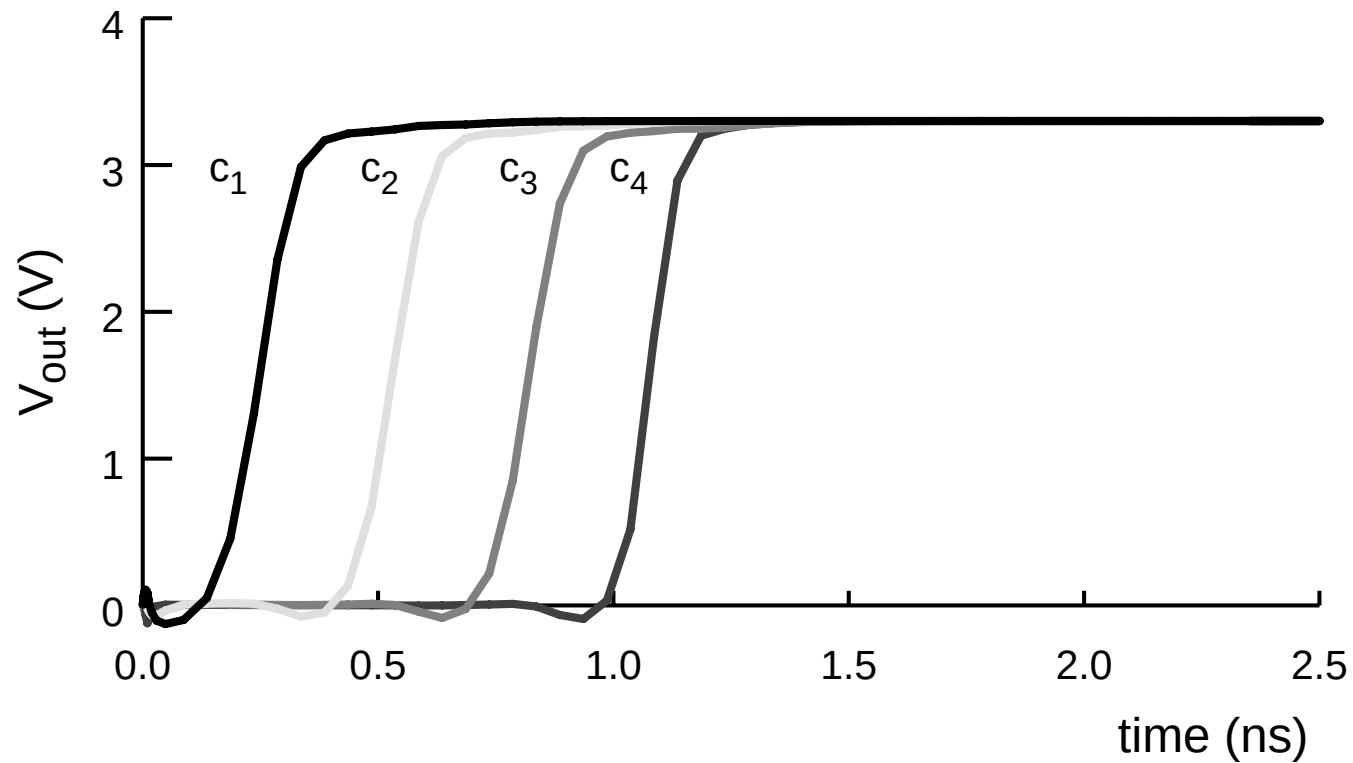
Case 1

W/L (in terms of μ , and not λ) for all stages: nmos = 0.75/0.5, pmos = 1.5/0.5



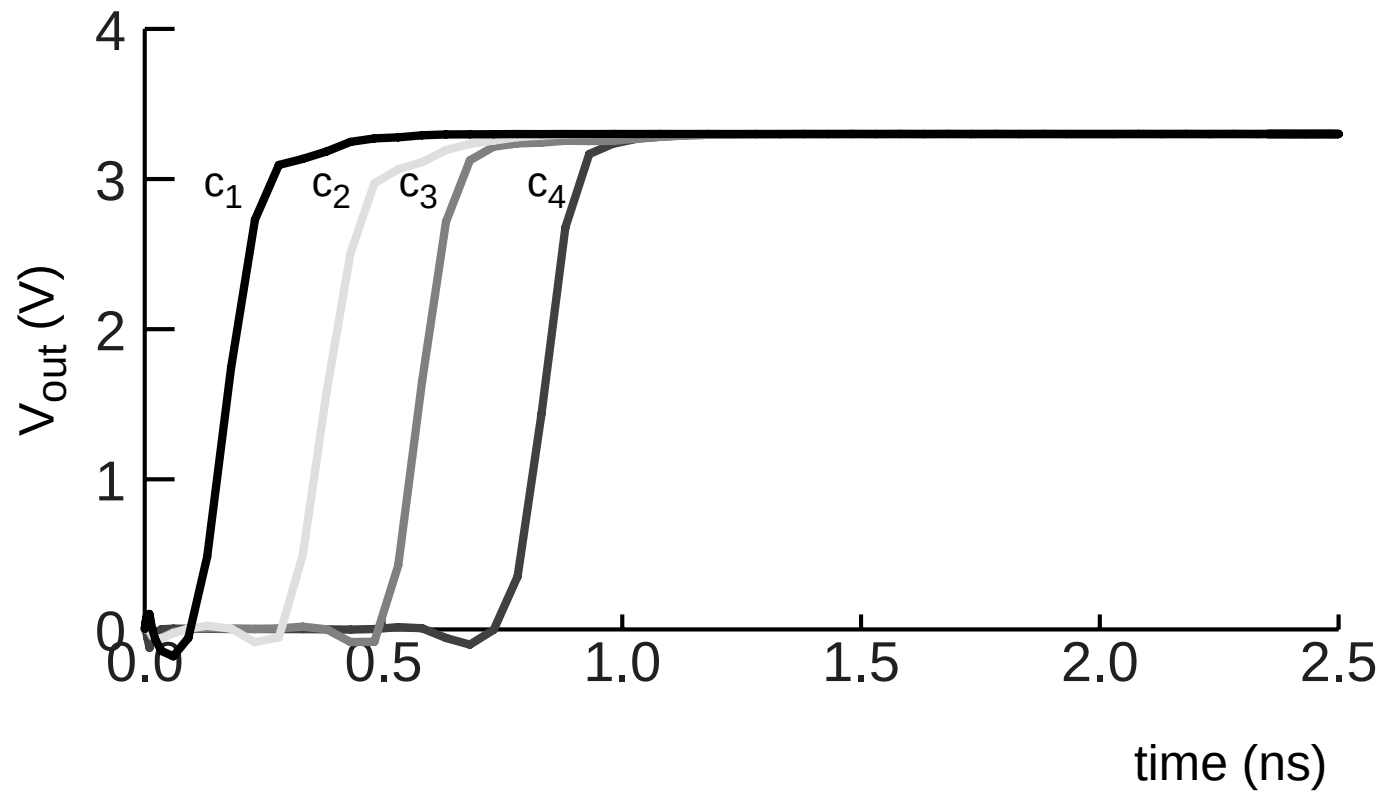
Case 2

Wider pulldowns for first stage, larger first stage inverter:



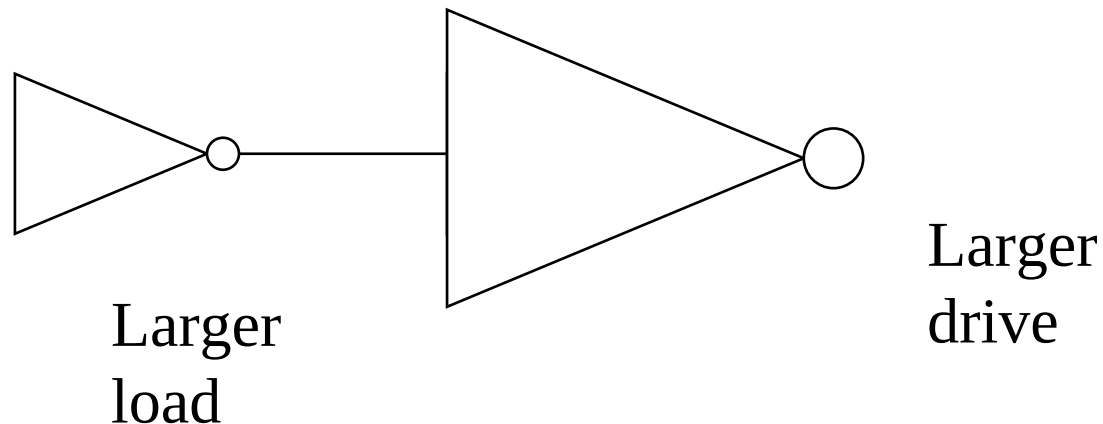
Case 3

Larger transistors in second and third stages:



Inter-stage effects in transistor sizing

- Increasing a gate's drive also increases the load to the previous stage:



Logical effort

- Logical effort is a gate delay model that takes transistor sizes into account.
- Allows us to optimize transistor sizes over combinational networks.
 - Isn't as accurate for circuits with reconvergent fanout.

Logical effort gate delay model

- Express delays in process-independent unit
- Gate delay is measured in units of minimum-size inverter delay τ .
$$d = \frac{d_{abs}}{\tau}$$
$$\tau = 3RC$$
$$\approx 12 \text{ ps in } 180 \text{ nm process}$$
$$40 \text{ ps in } 0.6 \mu\text{m process}$$
- Gate delay formula:
$$d = f + p.$$
- Effort delay f is related to gate's load.
- Parasitic delay p depends on gate's structure.
 - Represents delay of gate driving no load
 - Set by internal parasitic capacitance

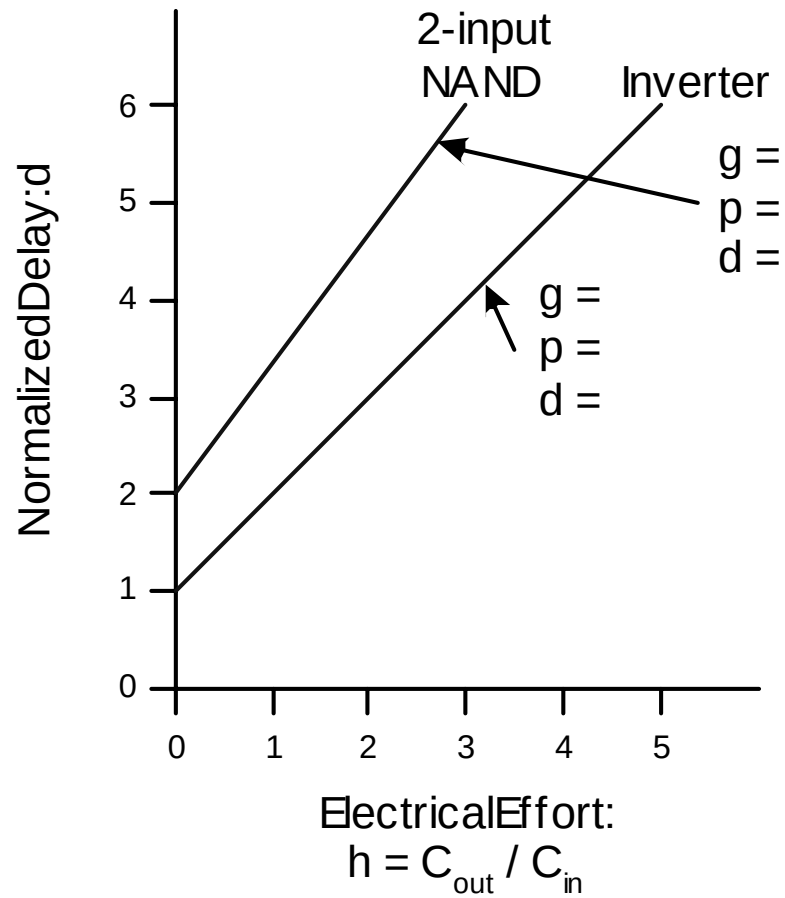
Effort delay

- Effort delay has two components:
 - $f = gh$.
- Electrical effort h is determined by gate's load:
 - $h = C_{out}/C_{in}$
 - Sometimes called fanout
- Logical effort g is determined by gate's structure.
 - Measures relative ability of gate to deliver current
 - $g \equiv 1$ for inverter

Delay Plots

$$d = f + p$$

$$= gh + p$$



Delay Plots

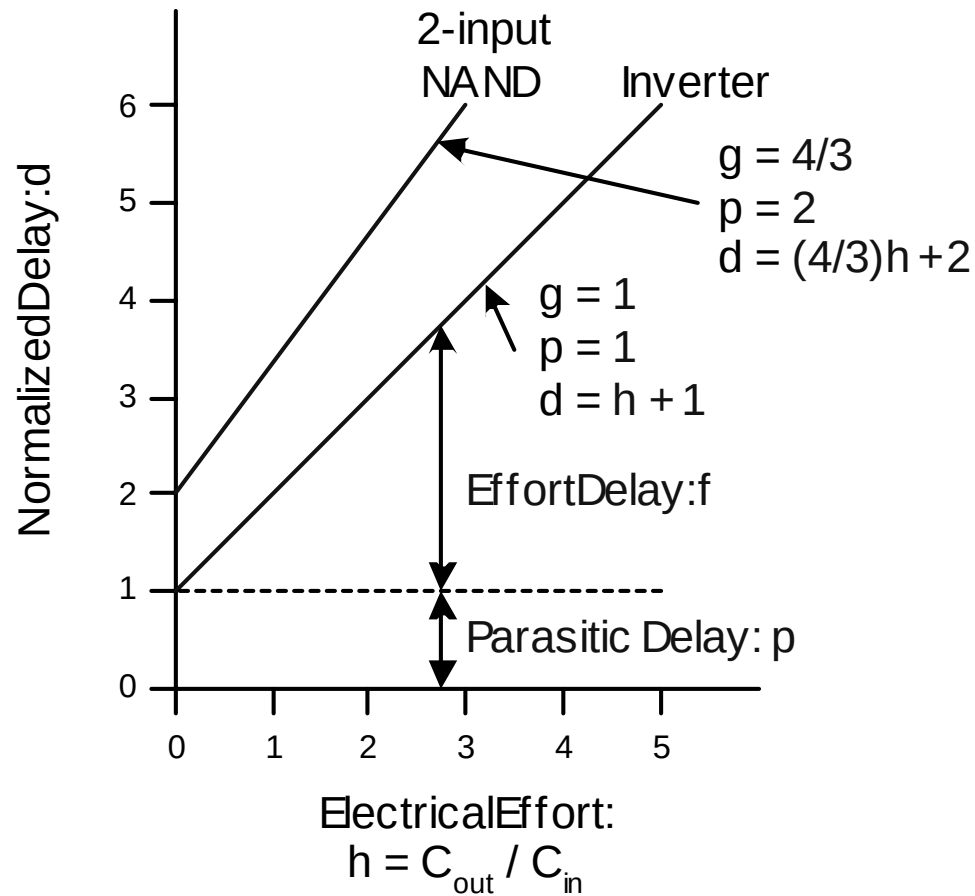
$$d = f + p$$

$$= gh + p$$

- What about NOR2?

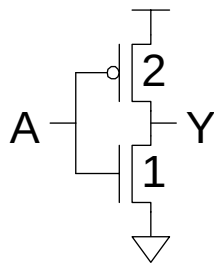
$$g = 5/3$$

$$h = 2$$

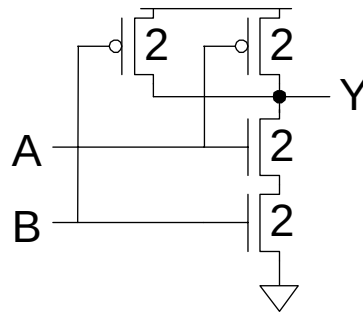


Computing Logical Effort

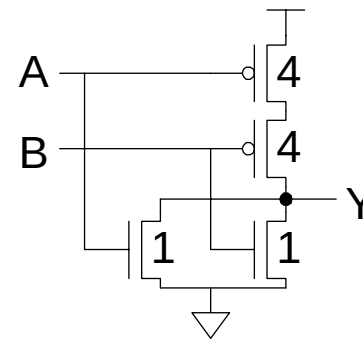
- *Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current.*
- Measure from delay vs. fanout plots
- Or estimate by counting transistor widths



$$C_{in} = 3$$
$$g = 3/3$$



$$C_{in} = 4$$
$$g = 4/3$$



$$C_{in} = 5$$
$$g = 5/3$$

Catalog of Gates

- Logical effort of common gates:

Gate type	Number of inputs				
	1	2	3	4	n
Inverter	1				
NAND		4/3	5/3	6/3	$(n+2)/3$
NOR		5/3	7/3	9/3	$(2n+1)/3$
Tristate / mux	2	2	2	2	2

Catalog of Gates

- Parasitic delay of common gates:
 - In multiples of p_{inv} (≈ 1)

Gate type	Number of inputs				
	1	2	3	4	n
Inverter	1				
NAND		2	3	4	n
NOR		2	3	4	n
Tristate / mux	2	4	6	8	2n

Logical effort along a path

- Logical effort along a chain of gates:
 - $G = \prod g_i$.
- Total electrical effort along path depends on ratio of first and last stage capacitances:
 - $H = C_{out}/C_{in}$.

Branching effort

- Takes into account fanout.
- Branching effort at one stage:

$$b = (C_{\text{onpath}} + C_{\text{offpath}}) / C_{\text{onpath}}$$

- Branching effort along path:

$$B = \prod b_i.$$

$$G = 1$$

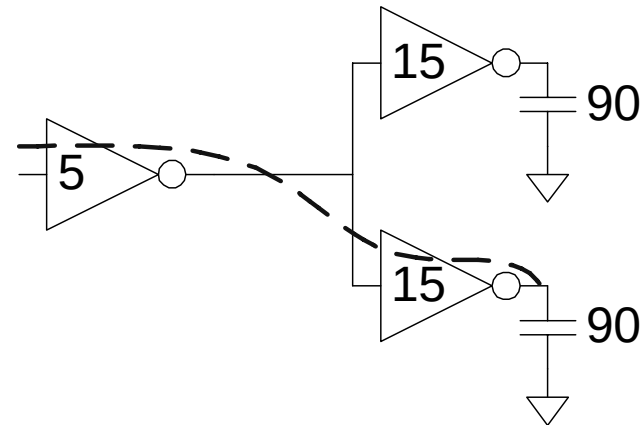
$$H = 90 / 5 = 18$$

$$GH = 18$$

$$h_1 = (15 + 15) / 5 = 6$$

$$h_2 = 90 / 15 = 6$$

$$F = g_1 g_2 h_1 h_2 = 36 = 2GH$$



Path delay

- Path effort:
 - $F = GBH$.
- Path delay is sum of delays of gates along the path:
 - $D = \sum g_i h_i + \sum p_i = D_F + P$.

Sizing the transistors

$$D = \sum d_i = D_F + P$$

- Delay is smallest when each stage bears same effort

- Optimal buffer chains are exponentially tapered:

$$\hat{f} = g_i h_i = F^{\frac{1}{N}}$$

- Thus minimum delay of N stage path is $D = NF^{\frac{1}{N}} + P$

- Determine W/L of each gate on path by working backward from the last gate:

$$\hat{f} = gh = g \frac{C_{out}}{C_{in}}$$

$$\Rightarrow C_{in_i} = \frac{g_i C_{out_i}}{\hat{f}}$$

Example: logical effort

- Size transistors in a chain of three two-input NAND gates.
 - First NAND is driven by minimum-size inverter.
 - Last NAND is connected to 4X inverter.

Example, cont'd.

- Logical effort $G = 4/3 * 4/3 * 4/3$.
- Branching effort = 1.
- Electrical effort = 4.
- $F = G B H = 9.5$.
- Optimum effort per stage $f^{\wedge} = 2.1$.